Amendment to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listings of Claims

Claims 1-6 (canceled)

Claim 7 (original): A semiconductor memory comprising:

a memory cell having ferroelectric capacitor which can be connected to a first bit line through a switching device;

a sense amplifier comparing an electric potential of said first bit line with a reference potential in order to read out data in said memory cell;

first and second dummy memory cells having ferroelectric capacitors which can be connected to a second bit line and a third bit line through switching devices in order to apply said reference potential to said sense amplifier; and

short-circuit means which short-circuits said second and third bit lines at the time of said data reading,

wherein said ferroelectric capacitors of both of said dummy memory cells are mutually polarized to opposite directions as storage information in the dummy memory cells, when the data is read out, the operation to apply the electric potentials from both of

said dummy memory cells to each bit line corresponding thereto is executed in a state where both of said second and third bit lines are mutually electrically shut off, and thereafter, an intermediate value of both electric potentials of both of said second and third bit lines which is obtained by said short-circuit of both of said second and third bit lines by said short-circuit means is supplied as a reference potential to said sense amplifier.

Claim 8 (original): A memory according to claim 7, wherein the polarizing directions of said ferroelectric capacitors of both of said dummy memory cells are sequentially reversed to the opposite directions every said data reading.

Claim 9 (original): A semiconductor memory comprising:

a memory cell having ferroelectric capacitor which can be connected to a first bit line through a switching device;

a sense amplifier comparing an electric potential of said first bit line with a reference potential in order to read out data in said memory cell;

first and second dummy memory cells having ferroelectric capacitors which can be connected to a second bit line and a third bit line through switching devices in order to apply said reference potential to said sense amplifier; and

short-circuit means which short-circuits said second and third bit lines at the time of said data reading,

wherein said ferroelectric capacitors of both of said dummy memory cells are mutually polarized to opposite directions as storage information in the dummy memory cells, and each time the data is read out, the polarizing directions of said ferroelectric capacitors of both of said dummy memory cells are sequentially reversed to the opposite directions.

Claim 10 (original): A memory according to claim 9, wherein an intermediate value of both electric potentials of said bit lines which are applied from said ferroelectric capacitors of both of said dummy memory cells to each of said bit lines corresponding thereto is supplied as a reference potential to said sense amplifier.

Claim 11 (original): A memory according to claim 9, wherein the operation to apply the electric potentials from both of said dummy memory cells to each bit line corresponding thereto is executed in a state where both of said second and third bit lines are mutually electrically shut off, and thereafter, an intermediate value of both electric potentials of both of said second and third bit lines which is obtained by the short-circuit of both of said second and third bit lines by said short-circuit means is supplied as a reference potential to said sense amplifier.